REMARKS

Present Status of the Application

The OFFICE ACTION rejected claims **1, 2,** and **4** under **35** U.S.C. **103(a)** as being unpatentable over Kammiller et al. (U.S. Patent# **5,619,405**) in combination with Lee (U.S. Patent # **5,644,214**). Claims **3,** and **5-24** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants have amended the claims to address minor informalities and more clearly define the invention.

Discussion of Office Action Rejections

Applicants much appreciate for the allowable subject matters that Examiner has indicated. In response to the rejected claims, Applicants would respectfully controvert as follows.

Firstly, Examiner indicated that item **66** in figure **2** of Kammiller et al is equivalent to the first multiplier-input (**VE**) of the present invention; item **76** in figure **2** of Kammiller et al is equivalent to the second multiplier-input terminal (**IAC**) of the present invention; item **60** in figure **2** of Kammiller et al is equivalent to the divisor-input terminal (**VAC**) of the present invention.

In traditional multiplier-dividers for power factor correction, the output signal is in proportion to the product of the line input current (I_{AC}) and the voltage error signal (V_E) divided by the square of the line input voltage (V_{AC}).

For corresponding relationship of Kammiller et al and the present invention, Applicants would respectfully clarify that the item **66**(line shape current) of Kammiller is not equivalent to the first multiplier-input (**VE**) of the present invention; that the item **76** (input current) of Kammiller et al is not equivalent to the second multiplier-input (**IAC**) of the present invention; and that the item **60** (voltage error signal) of Kammiller et al is not equivalent to the divisor-input (**VAC**) of the present invention.

Examiner further indicates that the present invention utilizes the similar technique taught by Lee (**5,644,214**) for a constant current source **135** (considered equivalent to the constant current **62** of Lee by Examiner) and a second multiplier-divider stage **150** (equivalent to the multiplier **48** of Lee by Examiner).

Applicants would respectfully controvert as follows.

The multiplier **48** of Lee multiplies the rectified input line voltage V_{in} and the output of the error amplifier **50** to generate an output voltage V_{mo} to be compared with the voltage V_{CS}. As V_{CS} is higher than V_{mo}, the switching element **64** is turned on for discharging the capacitor **66**. Therefore the control switch **22** is turned off and output regulation of the power converter is achieved.

In Lee, the output of the multiplier **48** is proportional to the product of two multiplier inputs. On the contrary, the second multiplier-divider **150** has an output, which in one embodiment is proportional to the product of two multiplier inputs divided by a divisor input. The multiplier **48** in Lee and the second multiplier-divider **150** are substantially different.

Compared to Lee, the present invention proposes two multiplier-divider stage cascaded using capacitor charging theory to obtain a desired output signal, which in one embodiment is proportional to the product of the voltage error signal V_E and the line input current I_{AC} divided by the square of the line input voltage V_{AC}. The constant current source **135** provides a constant current for the first multiplier-divider stage **130**. The output signal V_1 of the first multiplier-divider stage **130** is correlated to the magnitude of the constant current source **135**. However, the constant current source **62** of Lee is used to charge the capacitor **66** as the switching element **64** is off. The voltage across the capacitor **66** is utilized to control the control switch **22**.

In order to overcome the disadvantages of the prior art, the present invention proposes an innovative structure in (C)MOS process to resolve the problems of high cost, large die-space, temperature dependence of the prior arts.

For at least the reasons discussed above, claims 1, **2** and **4** are patentable over Kammiller and Lee.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims are in a proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 6/29/2005

Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809

Annotated Marked-up drawing

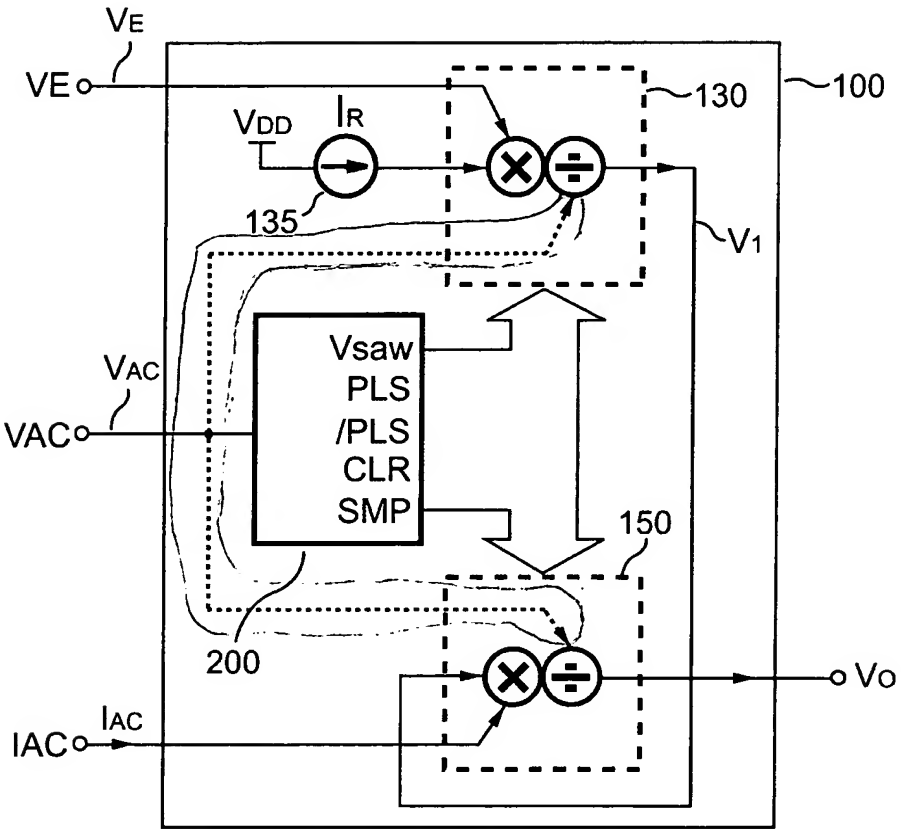

FIG. 3